REMARKS

Prior to this Reply, Claims 1-32 were pending in the above-referenced patent application. Though this Reply new Claims 33-34 have been added. As such, Claims 1-34 are now pending in the above-referenced patent application.

Claims 1, 4, 6-8, 17, 19, 21-25, 27 and 29-32 were rejected under 35 USC 102(e) as being anticipated by USPN 6,460,099 to Stryker et al ("Stryker"). Claims 2, 3, 5, 18, 20, 26 and 28 were rejected under 35 USC 103(a) as being unpatentable over Stryker in view of USPN 6,697,867 to Chong, Jr. ("Chong"). Claims 17-19, 21, 23-27, 29 and 31-32 were rejected under 35 USC 102(e) as being anticipated by Chong. Claims 9-12 and 15-16 were rejected under 35 USC 103(a) as being unpatentable over Chong in view of USPN 6,725,385 to Chu et al. ("Chu"). Claims 13 and 14 were rejected under 35 USC 103(a) as being unpatentable over Chong in view of Chu and further in view of Stryker. Claims 20, 22, 28 and 30 were rejected under 35 USC 103(a) as being unpatentable over Chong in view of Stryker.

At the outset, it is pointed out that in providing grounds for rejections of the Claims, the Office Action uses omnibus rejections, and broadly refers to lengthy passages in the references, which makes it difficult to understand and specifically respond to each rejection. Nevertheless, in the following, an attempt has been made to respond to all of the rejections. If the claims are once again rejected, it is respectfully requested that specific grounds for rejection of each claim be provided, and with more focused reference to the cited prior art.

Rejection of Claims 1, 4, 6-8, 17, 19, 21-25, 27 and 29-32 under 35 USC 102(e)

Rejection of Claims 1, 4, 6-8, 17, 19, 21-25, 27 and 29-32 under 35 USC 102(e) as being anticipated by Stryker is respectfully traversed because Stryker does not disclose all of the claimed limitations.

As per Claim 1, Stryker does not disclose: "a device controller that selectively activates at most two of the devices at the same time for data communication over the IDE bus," as required by Claim 1. By contrast, Stryker discloses selection of only one device for data communication over the IDE bus. Stryker (col. 4, lines 28-48, relied on by the Examiner) explicitly states: "Setting the CSEL line on an ATA mass storage device to a zero activates a drive. For this first method, only one mass storage device on the single ATA mass storage interface is allowed to be active at onetime." (col. 4, lines 36-39). There is no disclosure in Stryker col. 4, lines 28-48; col. 5, line 49 to col. 6, lines 24; Figs. 2A-B (relied on by the Examiner), or elsewhere, of connecting three or more devices to an IDE bus, configuring each device as Cable Select, and using *a device controller that activates two devices at the same time for data communication over the IDE bus*, as claimed herein. If the Examiner believes otherwise, it is respectfully requested that the Examiner specifically point to disclosure of such limitations in Stryker. For at least these reasons, rejection Claim 1 and all claims dependent therefrom should be withdrawn.

As per Claim 4, Stryker does not disclose: "the device controller is configured to activate a maximum of two of said three or more devices connected to the IDE bus at a time, and to deactivate the remaining of said three or more devices," as required by Claim 4. By contrast, as discussed above, Stryker discloses activation of only one device for data communication over the IDE bus. Further, in col. 4, lines (36-45 (relied on by the Examiner), Stryker states that: "Setting the CSEL line on an ATA mass storage device to a zero activates a drive. *For this first method, only one mass storage device on the single ATA mass storage interface is allowed to be active at onetime*. Setting the respective CSEL line high to make it a device 1 drive inactivates a drive. *The driver only accesses a device 0 drive, thus insuring that access to a device 1 drive does not occur.* Therefore in this first method, all drives are selectively enabled and accessed as device 0 drives and are disabled when configured as device 1 drives" (emphasis added). As this passage clearly states, Stryker discloses that only one device is active at a time --- only one device (device 0) is active.

There is no disclosure in Stryker of a device controller that allows two devices among multiple devices to be active at the same time for data communication over the IDE bus. For at least these reasons, rejection Claim 4 and all claims dependent therefrom should be withdrawn.

Claims 6-8 were rejected for essentially the same reasons as Claim 4, and should therefore be allowed for at least the reasons provided in relation to Claims 1 and 4.

As per Claim 17, Stryker does not disclose that: "the device controller selectively activates at most two of the devices at the same time for data communication with the processor over the IDE bus," as required by Claim 17. By contrast, Stryker discloses activation of only one device for data communication over the IDE bus. Stryker (col. 4, lines 28-48, relied on by the Examiner) explicitly states: "Setting the CSEL line on an ATA mass storage device to a zero activates a drive. For this first method, only one mass storage device on the single ATA mass storage interface is allowed to be active at onetime." (col. 4, lines 36-39). There is no disclosure in Stryker col. 4, lines 28-48; col. 5, line 49 to col. 6, lines 24; Figs. 2A-B (relied on by the Examiner), or elsewhere, of a device controller selectively activates at most two of the devices at the same time for data communication with the processor over the IDE bus, as claimed herein. Nor is there a disclosure in Stryker that a device driver as claimed is capable of receiving device control signals to select at least one of said devices for data communication with the processor. As discussed, Stryker's driver can select only one device on the IDE bus for data communication with a processor. For at least these reasons and the reasons provided in relation to Claim 1 and 4, rejection of Claim 17 and all claims dependent therefrom should be withdrawn.

Claim 25 was rejected for essentially the same reasons as Claim 17, and as such Claim 25 and all claims dependent therefrom should be allowed for at least the reasons provided in relation to Claims 17.

As per Claims 19 and 27, Stryker does not disclose a device controller that is configured to activate a maximum of two of said three or more devices connected to the IDE bus at a time, and to deactivate the remaining of said three or more devices, as required by Claims 19 and 27. By contrast, as discussed above, Stryker discloses activation of only one device for data communication over the IDE bus. Further, in col. 4, lines (36-45 (relied on by the Examiner), Stryker states that: "Setting the CSEL line on an ATA mass storage device to a zero activates a drive. *For this first method, only one mass storage device on the single ATA mass storage interface is allowed to be active at onetime*. Setting the respective CSEL line high to make it a device 1 drive inactivates a drive. *The driver only accesses a device 0 drive, thus insuring that access to a device 1 drive does not occur.* Therefore in this first method, all drives are selectively enabled and accessed as device 0 drives and are disabled when configured as device 1 drives" (emphasis added). As this passage clearly states, Stryker discloses that only one device is active at a time --- only one device (device 0) is active. There is no disclosure in Stryker of a device controller that allows two devices among multiple devices to be active at the same time for data communication over the IDE bus. For at least these reasons, rejection Claims 19, 27, and all claims dependent therefrom should be withdrawn.

Claims 21, 22, 24, 29, 30 and 32, were rejected for essentially the same reasons as Claims 6-8, and should therefore be allowed for at least the reasons provided in relation to Claims 1, 4, 6-8, 17 and 25.

As per Claims 23 and 31, Stryker does not disclose, an interface controller connected to said devices via the IDE bus, wherein the interface controller manages information flow between the processor and said devices over the IDE bus. The claimed interface controller acts as dedicated intermediary between the IDE device's internal controller and communication with the processor. The IDE interface controller manages the flow of information over an IDE bus, allowing the IDE devices to communicate with the processor. By contrast, Stryker (col. 7, lines 17-43, relied on by

the Examiner) describes a pair of subroutines in Figs. 5A-B, wherein the subroutine in Fig. 5A is called when the operating system requests access to an ATA mass storage device. Unlike the claimed interface controller herein, Stryker's subroutine is not required to be capable of managing information flow between the processor and the devices over the IDE bus. Stryker's subroutine is simply a queue handler, and is not for information flow between the processor and IDE devices *over the IDE bus*, as claimed. Further, Stryker specifically states: "The subroutine does a check in block 152 to see if the subroutine supports the device that is being requested. If not, the subroutine returns control to the operating system in block 154" (Stryker, col. 7, lines 19-23). This is in contrast to the claimed interface controller that is required to manage information flow between the processor and the devices over the IDE bus. For at least these reasons, rejection Claims 23 and 31 should be withdrawn.

Rejection of Claims 2, 3, 5, 18, 20, 26 and 28 under 35 USC 103(a)

Rejection of Claims 2, 3, 5, 18, 20, 26 and 28 under 35 USC 103(a) as being unpatentable over Stryker in view of Chong is respectfully traversed because the references, alone or in combination, do not disclose all of the claimed limitations.

As per Claim 2, 3, 18 and 26, as discussed above, Stryker fails to disclose all of the limitations of the base Claims 1 and 17. Further, as the Examiner also states, Stryker fails to disclose a device controller with features of: identifying one or two devices for data communication with the processor, selecting a first of the identified devices as a master device, if more than one device identified, then selecting the second of the identified devices as a slave device, and activating each selected device, such that a maximum of only two devices are active at the same time, whereby the activated devices can communicate with the processor over the IDE bus, as required by Claims 2 and 18. However, the Examiner interprets Chong to disclose such limitations. This interpretation of Chong is respectfully traversed.

In col. 6, lines 1-65 and Fig. 1 (relied on by the Examiner) there is no disclosure in Chong of identifying one or two devices, among three or more devices on the IDE bus, for data communication with the processor, as required by Claims 2 and 18. In Chong there are only two ATA devices in either 21A or 21B (Fig. 1), whereby there is no need or disclosure in Chong for a step of identifying among three or more devices on the IDE bus which are active at the same time, as claimed.

Further, there is no need or disclosure in Chong for the decision step: if more than one device is identified, then selecting the second of the identified devices as a slave device, as required by Claims 2 and 18. Because as discussed there is no identification step in Chong, there is no need or disclosure for checking if more than one device has been identified. And, as such, there is no need or disclosure for *selecting* a second identified device, among three or more devices on the same IDE bus, as a slave. For that matter, there is no disclosure in Chong of selecting a first identified device among three or more devices on the IDE bus, as a master.

Further, Chong does not disclose: activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, as required by Claims 2 and 18. Though Chong mentions master/slave selection, Chong is silent on activating selected devices such that they are active at the same time. This allows the activated devices to communicate with the processor over the IDE bus, as required by Claims 2 and 18.

Indeed, Chong teaches away from the claimed limitations. In col. 6, lines 54-63 (relied on by the Examiner) Chong states: "*As an example of accessing a particular device, in order to access ATA device 20C*, the second value may be stored in control register 26. In response to the second value, signal routing logic 24 produces signals CS0B and CS1B having the same logical values as respective signals CS0 and CS1. ATA devices 20C and 20D are thus selected, and *other signals ... may be used to select ATA device 20C from the master/slave pair including ATA devices*

20C and 20D." (emphasis added). This is in distinct contradiction with the claimed limitations of: activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, as required by Claims 2 and 18.

There is no suggestion or motivation in either Stryker or Chong to combine them. It is well settled that in order for a modification or combination of the prior art to be valid, the prior art itself must suggest the modification or combination, "...invention cannot be found obvious unless there was some **explicit** teaching or suggestion in the art to motivate one of ordinary skill to combine elements so as to create the same invention." *Winner International Royalty Corp. v. Wang*, No. 96-2107, 48 USPQ.2d 1139, 1140 (D.C.D.C. 1998) (emphasis added). "The prior art **must provide** one of ordinary skill in the art the **motivation** to make the proposed molecular modifications needed to arrive at the claimed compound." *In re Jones*, 958 F.2d 347, 21 USPQ.2d 1941, 1944 (Fed. Cir. 1992) (emphasis added). As there is no suggestion or motivation in either Stryker or Chong to combine them, the modification suggested by the Examiner is legally not justified.

As discussed, Stryker is explicit that only one mass storage device on the single ATA mass storage interface is allowed to be active at one time. There is no motivation in Stryker to change that. The Examiner states that Chong suggests use of plural master/slave groups in col. 1, lines 26-28 and col. 2 lines 7-46. However, in col. 2, lines 7-46, Chong only refers to the basis ATA standard. And, in col. 2, lines 7-46, Chong simply provides a summary of the invention therein (i.e., system and method for accessing multiple groups of peripheral devices) without any suggesting/motivation of any one of the claimed limitations: placing three or more IDE devices on an IDE bus, identifying one or two devices for data communication with the processor, selecting a first of the identified devices as a master device, if more than one device identified, then selecting the second of the identified devices as a slave device, and activating each selected device, such that a maximum of only two devices are active at the same time, whereby the activated devices can

communicate with the processor over the IDE bus, as required by Claims 2 and 18.

Even if the modification was legally justified, it still would not render Applicants' claimed invention obvious. The Patent Office admits that Stryker does not teach all limitations in Claims 2 and 18. Therefore, the Patent Office attempts to modify Stryker in order to teach Applicant's claimed invention. However, as discussed, there is no teaching in Chong of the claimed limitations. It is respectfully submitted that that the Patent Office has not meet its burden of establishing a prima facie case of obviousness. The effort required to combine the teachings of Stryker and Chong would require a substantial undertaking and numerous elements which would not be obvious. The Patent Office is improperly using "hindsight" and the teachings of Applicant's own claimed invention in order to combine references to render Applicant's claims obvious. The Patent Office Action admits that Stryker fails to teach all of the limitations of Applicant's claimed invention. However, the Patent Office improperly attempts to modify Stryker in an attempt to achieve Applicant's claimed invention. For at least these reasons, rejection of Claims 2, 18 and all claims dependent therefrom should be withdrawn.

As per Claims 5, 20 and 28, as discussed Stryker does not disclose all of the limitations of the base Claims 1, 17 and 25. Further, as the Examiner also states neither Stryker nor Chong disclose that the device controller is configured to activate said maximum of two devices by powering the two devices on, and to deactivate said remaining devices by powering said remaining devices off, as required by Claims 5, 20 and 28. However, the Examiner concludes that such limitations are obvious without providing any support in the prior art. No prima facie case of obviousness has been established. There is no disclosure, suggestion or motivation in the cited references (alone or in combination) of activating two devices on the IDE bus at the same time, as claimed herein. There is no disclosure, suggestion or motivation in the cited references (alone or in combination) of and to deactivate said remaining devices by powering said remaining devices off, as claimed herein. Surely, if such limitations were obvious, then Stryker and/or Chong (which the

Examiner has relied on in rejection of the claims) would have disclosed such limitations. Nor is there any suggestion, discussion or motivation in the cited references about saving power as the Examiner suggests. It is well settled that in order for a modification or combination of the prior art to be valid, the prior art itself must suggest the modification or combination. For at least theses reasons, rejection of Claims 5, 20 and 28 should be withdrawn.

Rejection of Claims 17-19, 21, 23-27, 29 and 31-32 under 35 USC 102(e)

Rejection of Claims 17-19, 21, 23-27, 29 and 31-32 under 35 USC 102(e) as being anticipated by Chong is respectfully traversed because Chong does not disclose all of the claimed limitations.

As per Claims 17 and 25, it is respectfully submitted that Chong fails to disclose that a device controller selectively activates at most two of the devices at the same time for data communication with the processor over the IDE bus, as claimed. Though Chong mentions master/slave selection, Chong is silent on activating selected devices such that they are active at the same time. In col. 5, lines 13-44 (relied on by the Examiner) Chong mentions selecting between 21A and 21B in Fig. 1, but no mention of activating at most two of the devices at the same time for data communication with the processor over the IDE bus, as claimed. Indeed, Chong teaches away from the claimed limitations. In col. 6, lines 54-63, Chong states: "As an example of accessing a particular device, in order to access ATA device 20C, the second value may be stored in control register 26. In response to the second value, signal routing logic 24 produces signals CS0B and CS1B having the same logical values as respective signals CS0 and CS1. ATA devices 20C and 20D are thus selected, and other signals ... may be used to select ATA device 20C from the master/slave pair including ATA devices 20C and 20D." This is in distinct contradiction with the claimed limitations of a device controller selectively activates at most two of the devices at the same time for data communication with the processor over the IDE bus, as claimed, as claimed. For at least these reasons, rejection of Claims 17, 25 and all claimed dependent therefrom should be

withdrawn.

As per Claims 18, 19, 21, 23, 24, 26, 27, 29, 31 and 32, as dicussed, Chong fails to disclose limitations of base claims 17 and 25. Further, Chong fails to disclose a device controller with features of: identifying one or two devices for data communication with the processor, selecting a first of the identified devices as a master device, if more than one device identified, then selecting the second of the identified devices as a slave device, and activating each selected device, such that a maximum of only two devices are active at the same time, whereby the activated devices can communicate with the processor over the IDE bus, as required by Claims 18 and 26. In col. 6, lines 1-65 and Fig. 1 (relied on by the Examiner) there is no disclosure in Chong of identifying one or two devices, among three or more devices on the IDE bus, for data communication with the processor, as required by Claims 2 and 18. In Chong there are only two ATA devices in either 21A or 21B (Fig. 1), whereby there is no need or disclosure in Chong for a step of identifying among three or more devices on the IDE bus which are active at the same time, as claimed.

Further, there is no need or disclosure in Chong for the decision step: if more than one device is identified, then selecting the second of the identified devices as a slave device, as required by Claims 2 and 18. Because as discussed there is no identification step in Chong, there is no need or disclosure for checking if more than one device has been identified. And, as such, there is no need or disclosure for *selecting* a second identified device, among three or more devices on the same IDE bus, as a slave. For that matter, there is no disclosure in Chong of selecting a first identified device among three or more devices on the IDE bus, as a master.

Further, Chong does not disclose: activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, as required by Claims 2 and 18. Though Chong mentions master/slave selection, Chong is silent on activating

selected devices such that they are active at the same time. This allows the activated devices to communicate with the processor over the IDE bus, as required by Claims 18 ands 26.

Indeed, Chong teaches away from the claimed limitations. In col. 6, lines 54-63 (relied on by the Examiner) Chong states: "As an example of accessing a particular device, in order to access ATA device 20C, the second value may be stored in control register 26. In response to the second value, signal routing logic 24 produces signals CS0B and CS1B having the same logical values as respective signals CS0 and CS1. ATA devices 20C and 20D are thus selected, and other signals ... may be used to select ATA device 20C from the master/slave pair including ATA devices 20C and 20D." This is in distinct contradiction with the claimed limitations of: activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, as required by Claims 18 and 26. For at least theses reasons, rejection of Claims 18 and 26 should be withdrawn.

As per Claims 19 and 27, Chong does not disclose that a device controller is configured to activate a maximum of two of said three or more devices connected to the IDE bus at the same time, and to deactivate the remaining of said three or more devices, as claimed. In col. 6, lines 54-63 (relied on by the Examiner) Chong states: "As an example of accessing a particular device, in order to access ATA device 20C, the second value may be stored in control register 26. In response to the second value, signal routing logic 24 produces signals CS0B and CS1B having the same logical values as respective signals CS0 and CS1. ATA devices 20C and 20D are thus selected, and other signals ... may be used to select ATA device 20C from the master/slave pair including ATA devices 20C and 20D." This is in distinct contradiction with the claimed limitations of activating two of said three or more devices connected to the IDE bus at the same time. For at least these reasons, rejection of Claims 19 and 27 should be withdrawn.

As per Claims 23 and 31, Chong, col. 1, lines 13-25 and col. 5, lines 13-44 (relied on by the

Examiner) does not disclose an interface controller connected to said devices via the IDE bus, wherein the interface controller manages information flow between the processor and said devices over the IDE bus, as required by Claims 23 and 31. In col. 1, lines 13-25, Chong simply mention various prior art ATA devices, which have nothing to do with the claimed limitation. Further, in col. 5, lines 13-44, Chong describes various selection signals for selecting a single ATA device in 21A or 21B (Fig. 1). There is no mention there on an interface controller that manages information flow between the processor and said devices over the IDE bus, as claimed. There is no interface device discussed or suggested in Chong. The Examiner has not pointed to a disclosure of such limitations in Chong. Further, because as in Stryker, Chong activates a single ATA device, there is no need for a specialized interface controller as claimed, to manage information flow between the processor and devices over the IDE bus which can be active at the same time. For at least these reasons, rejection of Claims 23 and 31 should be withdrawn.

Rejection of Claims 9-12 and 15-16 under 35 USC 103(a)

Rejection of Claims 9-12 and 15-16 under 35 USC 103(a) as being unpatentable over Chong in view of Chu is respectfully traversed because the references, alone or in combination, do not disclose all of the claimed limitations.

As per Claim 9, in col. 6, lines 1-65 and Fig. 1 (relied on by the Examiner), or elsewhere in Chong, there is no disclosure of identifying one or two devices, among three or more devices on the IDE bus, for data communication with the processor, as claimed. In Chong there are only two ATA devices in either 21A or 21B (Fig. 1), whereby there is no need or disclosure in Chong for a step of identifying among three or more devices on the IDE bus which are active at the same time, as claimed. Further, there is no need or disclosure in Chong for the decision step: if more than one device is identified, then selecting the second of the identified devices as a slave device, as required by Claims 2 and 18. Because as discussed there is no identification step in Chong, there is no need or disclosure for checking if more than one device has been identified. And, as such, there is no

need or disclosure for *selecting* a second identified device, among three or more devices on the same IDE bus, as a slave. For that matter, there is no disclosure in Chong of selecting a first identified device among three or more devices on the IDE bus, as a master.

Further, Chong does not disclose: activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, as claimed. Though Chong mentions master/slave selection, Chong is silent on activating selected devices such that they are active at the same time. This allows the activated devices to communicate with the processor over the IDE bus, as claimed. Indeed, Chong teaches away from the claimed limitations. In col. 6, lines 54-63 (relied on by the Examiner) Chong states: "*As an example of accessing a particular device, in order to access ATA device 20C*, the second value may be stored in control register 26. In response to the second value, signal routing logic 24 produces signals CS0B and CS1B having the same logical values as respective signals CS0 and CS1. ATA devices 20C and 20D are thus selected, and *other signals ... may be used to select ATA device 20C from the master/slave pair including ATA devices 20C and 20D.*" (emphasis added). This is in distinct contradiction with the claimed limitations of: activating each selected device, such that a maximum of only two devices among said three or more devices are active at the same time, as required by Claim 9.

Further, as the Examiner also states, Chong does not disclose a method for communicating data between a processor and three or more devices over an IDE bus by first deactivating all the devices, as required by Claim 1. However, the Examiner interprets Chong, col. 2, lines 25-34, and Chu to disclose such a limitation. These interpretations of Chong and Chu are respectfully traversed.

In col. 2, lines 25-34 (relied on by the Examiner), Chong simply mentions: "The signal routing logic receives an access signal from the host system and routes the access signal to the

group access signal for the group of peripheral devices selected by the value stored in the control register. The group access signal for each of the remaining groups of peripheral devices is deasserted so that the groups of peripheral devices not selected by the value stored in the control register are not accessed (i.e., do not respond to accesses from the host system)." In this passage, or elsewhere in Chong, there is not single word about activating or deactivating any devices. Nor is there any disclosure or need in Chong about deactivating any of the devices since Chong uses device selection for accessing a single device (as discussed above). The Examiner's interpretation of Chong is respectfully traversed.

Further, Chu has nothing to do with the present invention Chu is directed to a device connected to an interface has operational logic and power control logic. The device further has multiple power modes, including a first mode and a second, lower power mode. In the first mode, the operational logic is coupled to the interface, and is able to communicate over the interface. In the second mode, the power control logic is coupled to the interface, and the operational logic is decoupled, and substantially powered down. This provides a low interface power mode. In this mode, the power control logic monitors the interface for command activity. The power control logic returns the device to the first mode when the device must be in the first mode to process or reply to the command. The power control logic thus provides for the restoration of function from a low interface power mode without the need for a special "wake-up" command, thereby making the low interface power mode transparent to the host (Abstract).

There is no mention or suggestion in Chu of connecting three or more IDE devices to an IDE bus, to extend capability of an IDE bus according to the present invention. Chu is entirely concerned with power consumption and a power controller to control interface power consumption of a device so that the device power consumption is reduced from that in low-power modes of the devices (col. 1, lines 54-57). Indeed, Chu is non-analogous art.

Further, Despite the Examiner's assertion, it is respectfully submitted that Applicant cannot find any teaching in Chu, col. 1, lines 13-53, col. 2, lines 12-30, col. 3, lines 45-67 (relied on by the Examiner), of deactivating all of the devices on an IDE bus. If the Examiner believes otherwise, Applicant respectfully requests a quotation from Chu where such limitations are disclosed.

In col. 1, lines 13-19 (relied on by the Examiner), Chu simply mentions various power modes of HDDs, wherein in every mode at least a part of the HDD is powered. This has nothing to do with the claimed limitations of deactivating all of the devices. Chu, col. 1, lines 13-19, states: "Hard Disk Drives (HDDs) have multiple power modes that trade-off energy consumption for response time. Accordingly, a relatively short response time has an associated relatively higher energy consumption because a greater proportion of the HDD is powered up and active. Typical power modes for an HDD include Active, Idle, Standby and Sleep modes. Other mobile computer peripheral devices, such as a microprocessor (μP) and a liquid crystal display (LCD), provide power modes that are analogous to HDD power modes." As such, unlike the claimed limitations, according to Chu, in various power modes at least a part of the device is powered. There is no disclosure in Chu of all devices on an IDE bus being deactivates, as claimed.

It is well settled that in order for a modification or combination of the prior art to be valid, the prior art itself must suggest the modification or combination. There is no motivation or suggestion, motivation or need in Chong for saving power as the Examiner suggests. Chu is only concerned about reducing power consumption, and in no way related to a method for communicating data between a processor and three or more devices over an IDE bus, as claimed. There is no motivation or suggestion in either reference to combine them. Even if Chong is modified according to Chu as the Examiner suggests, the resulting system is one in which the IDE devices may operate at lower power levels, but will not be deactivated. At any rate, a deactivation of all of the IDE devices in Chong would be disruptive to Chong's selecting circuit. Further, even if all of the devices in Chong are deactivated, there is no disclosure anywhere in Chong that such a

deactivation allows Chong to select more than one device at a time. Accordingly, any modification of Chong using Chu as suggested by the Examiner, still does not disclose the claimed limitations. There is no disclosure in the references, alone or in combination, of deactivating all of the devices, selecting one or more devices, and activating at most two selected devices at the same time to communication with a processor.

Controlling power consumption of devices has nothing to do with the claimed limitations of deactivating all of the devices, and reactivating selected devices as part of a method for communicating data between a processor and three or more devices over an IDE bus, as claimed. For at least these reasons, rejection of Claim 9 and all claims dependent therefrom should be withdrawn.

As per Claim 10, for at least the reasons provided in relation to Claim 9, the references alone or in combination do not disclose the step of deactivating all of the devices after communication between the processor and each activated device.

As per Claim 11, for at least the reasons provided in relation to Claims 9 and 10, the references alone or in combination do not disclose repeating the process of deactivating all of the devices, selecting one or more devices, and activating at most two selected devices at the same time to communication with a processor.

As per Claim 15, for at least the reasons provided in relation to Claim 9, despite the Examiner's assertion, the references alone or in combination do not disclose powering off all devices, and then powering on selected devices. In Chu, col. 6, lines 21-65 (relied on by the Examiner) there is not a single word about powering off all devices. Nor is there any word about powering on selected devices. If the Examiner believes otherwise, Applicant respectfully requests a specific reference or quotation in Chu, rather than broad reference to lengthy sections of Chu that

have nothing to do with the claimed limitations. Further, Chu does not power devices on and off, rather Chu controls how much power is supplied to the devices without powering them off. For at least these reasons, rejection of Claim 15 should be with withdrawn.

Rejection of Claims 13-14 under 35 USC 103(a)

Rejection of Claims 13 and 14 under 35 USC 103(a) as being unpatentable over Chong in view of Chu and further in view of Stryker is respectfully traversed because the references, alone or in combination, do not disclose all of the claimed limitations.

As per Claims 13 and 14, as discussed, Chong and Chu, alone or in combination, do not disclose all of the limitations of base Claim 9. As per Claim 13, as the Examiner also states, Chong and Chu do not disclose the limitation of configuring each device as Cable Select, before deactivating the devices, as claimed. However, the Examiner asserts that Stryker discloses such a limitation. Indeed, Stryker fails to disclose Cable Select configuration of the devices before deactivation, since Stryker does not deactivate any of the devices. For at least these reasons, rejection of Claim 13 should be withdrawn.

As per Claim 14, as the Examiner also states, Chong and Chu do not disclose the limitations of: selecting the first identified device as a master device via the Cable Select signal for that first device, and selecting the second identified device as a slave device via the Cable Select signal for that second device. Stryker, in col. 3, lines 25-28, col. 4, lines 28-38 and col. 7, lines 17-43 (relied on by the Examiner) discloses CSEL signals for selecting a single device for access, not two devices at the same time. Further, unlike the claimed limitations, the CSEL signals in Stryker are utilized when the devices are active. By contrast, as claimed herein, the Cable Select signals are asserted when the devices are inactive.

There is no motivation or suggestion in the references to combine them. The Examiner's

stated motivation for combining the references is lacking, because according to the Examiner's prior interpretation of the references, Chong and Stryker are able to provide dynamic selection of a first device as master and a second device as slave, while those devices are active. In other words, even according to Examiner's prior interpretation of the references in their ability to select a device for access, no changes to Chong or Stryker in the form of first deactivating the devices, and then activating master and slave devices after Cable Select settings, are needed in to enable such dynamic selection. Further, activation/deactivation as claimed (i.e., power on/off), and that in Stryker and Chong (selection/deselection, assertion/deassertion) are different concepts.

Even if Chong, Chu and Stryker can be legally combined, the result still does not disclose the claimed limitations of setting the Cable Select signals for selected devices while the devices are inactive, and then activating the selected devices after the Cable Select signals are set. For at least these reasons, rejection of Claim 14 should be withdrawn.

Rejection of Claims 20, 22, 28 and 30 under 35 USC 103(a)

Rejection of Claims 20, 22, 28 and 30 under 35 USC 103(a) as being unpatentable over Chong in view of Stryker is respectfully traversed because the references, alone or in combination, do not disclose all of the claimed limitations.

As per Claims 20 and 28, as dicussed the references do not disclose limitations of base claims 17, 19 and 25, 27. As the Examiner also states, Chong and Stryker fail to disclose that a device controller is configured to activate said maximum of two devices by powering the two devices on, and to deactivate said remaining devices by powering said remaining devices off. However, the Examiner concludes that such limitations are obvious, without providing any support in the prior art. No prima facie case of obviousness has been established. There is no disclosure, suggestion or motivation in the cited references (alone or in combination) of activating maximum of two devices by powering the two devices on, and to deactivate said remaining devices by powering

said remaining devices off. Surely, if such limitations were obvious, then Stryker and/or Chong (which the Examiner has relied on in rejection of the claims) would have disclosed such limitations. Nor is there any suggestion, discussion or motivation in the cited references about saving power as the Examiner suggests. Further, as discussed, power saving has nothing to do with the claimed limitations of deactivating all of the devices, and reactivating selected devices as part of a method for communicating data between a processor and three or more devices over an IDE bus, as claimed. The Examiner has not shown any disclosure in the references, nor presented any basis, showing that the references power devices on/off. The Examiner has not shown any disclosure in the references, nor presented any basis, that powering devices on/off as claimed herein is disclosed in the references as a method for communicating data between a processor and one or more devices over an IDE bus, as claimed herein. Indeed, in the references, powering devices on/off to save power will directly interfere with the operations of the systems described therein. For at least these reasons, rejection of Claims 20, 28 and all claims dependent therefrom should be withdrawn.

New Claims

New Claims 33 and 34 claim further limitations of using a USB bus for connecting drives to the processor, as described in the originally filed description, which limitations are not disclosed by the references alone or in combination.

CONCLUSION

For the foregoing, and other, reasons Applicants believe that the rejected claims should be allowed. Reconsideration and allowance of the rejected claims are respectfully requested.

Please continue to direct all communications regarding the above-referenced patent application to the principal agent of record.

Respectfully Submitted,

Michael Zarrabian
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CERTIFICATE OF MAILING

I hereby certify that this correspondence or paper is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, on April 13, 2005.

By_____
Signature

Michael Zarrabian
Typed Name of Person Mailing Paper or Fee